APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM
37 C.F.R. § 1.121(b)(ii) AND (c)(i)

CLAIMS (with indication of amended or new):

9. (Four Times Amended) The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

10. (Amended) The process of claim 9, wherein said polysilicon stripes have a width of 3.1 microns and a spacing of 1.25 microns.

11. (Amended) The process of claim 9 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

12. (Amended) The process of claim 10 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

13. (Amended) The process of claim 9 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter

depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

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14. (Amended) The process of claim 12 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.